What is claimed is:

1. A method of operation in a system that includes a first integrated circuit device and a second integrated circuit device, the method comprising:

transmitting a data sequence from the first integrated circuit device to the second integrated circuit device;

sampling the data sequence by the second integrated circuit device to produce receiver data;

transmitting the receiver data from the second integrated circuit device to the first integrated circuit device;

performing a comparison, within the first integrated circuit device, between the data sequence and the receiver data; and

based on the comparison, generating information representative of a calibrated timing offset; and

using the information representative of the calibrated timing offset to adjust timing associated with transferring write data from the first integrated circuit to the second integrated circuit.

2. The method of claim 1 further including storing the receiver data in the second integrated circuit.

3. The method of claim 1 further including adjusting transmission timing of the write data by the first integrated circuit based on the information representative of the calibrated timing offset.

4. The method of claim 1 further including adjusting timing of sampling of the write data by the second integrated circuit based on the information representative of the calibrated timing offset.

5. The method of claim 1, wherein the method is performed as part of a calibration sequence.

6. The method of claim 5, wherein the method is performed periodically.

7. The method of claim 5, wherein the method is performed during initialization of the system.

8. The method of claim 1, wherein the calibrated timing offset is an offset relative to a master clock that is received by the second integrated circuit.

9. The method of claim 1, wherein the first integrated circuit is a controller device and the second integrated circuit device is a memory device, and wherein the method further comprises performing write operations to the memory device using the information representative of a calibrated timing offset.

10. The method of claim 1, wherein

said transmitting of the data sequence from the first integrated circuit device to the second integrated circuit device includes transmitting a calibration clock signal that is shifted by about 90° with respect to main clock signal; and

said method includes transmitting write data from the first integrated circuit to the second integrated circuit in conjunction with transmitting said main clock signal.

11. The method of claim 10, wherein said transmitting, sampling, transmitting and performing a comparison are repeated a plurality of times, using a plurality of different timing offsets, said generating information representative of a calibrated timing offset including identifying a timing offset associated with a change in the receiver data compared with the receiver data at another timing offset.

12. The method of claim 1, wherein said transmitting, sampling, transmitting and performing a comparison are repeated a plurality of times, using a plurality of different timing offsets, said generating information representative of a calibrated timing offset including identifying first and second timing offsets associated with opposing edges of a data eye, and wherein the calibrated timing offset is an offset between the first and second timing offsets.

13. A system comprising a first integrated circuit device and a second integrated circuit device and a signal path connecting the first integrated circuit device to the second integrated circuit device;

the first integrated circuit device including a transmitter configured to transmit a data sequence to the second integrated circuit device;

the second integrated circuit device including a receiver configured to sample the data sequence to produce receiver data, and a transmitter configured to transmit the receiver data to the first integrated circuit device;

wherein the first integrated circuit device is further configured:

to perform a comparison between the data sequence and the receiver data;

based on the comparison, to generate information representative of a calibrated timing offset; and

to use the information representative of the calibrated timing offset to adjust timing associated with transferring write data from the first integrated circuit to the second integrated circuit.

14. The system of claim 13, wherein the second integrated circuit device includes a register to store the calibrated timing offset.

15. The system of claim 14, wherein the second integrated circuit device includes a locked loop circuit to generate a receive clock signal in accordance with the calibrated timing offset stored in the register.

16. The system of claim 13, wherein the first integrated circuit device includes a register to store the calibrated timing offset.

17. The system of claim 16, wherein the first integrated circuit device includes a locked loop circuit to generate a transmit clock signal in accordance with the calibrated timing offset stored in the register.